



IBM Haifa Research Lab

Bridging Pre-Silicon Verification and Post-Silicon Validation and Debug

A Pre-Silicon Functional Verification Perspective

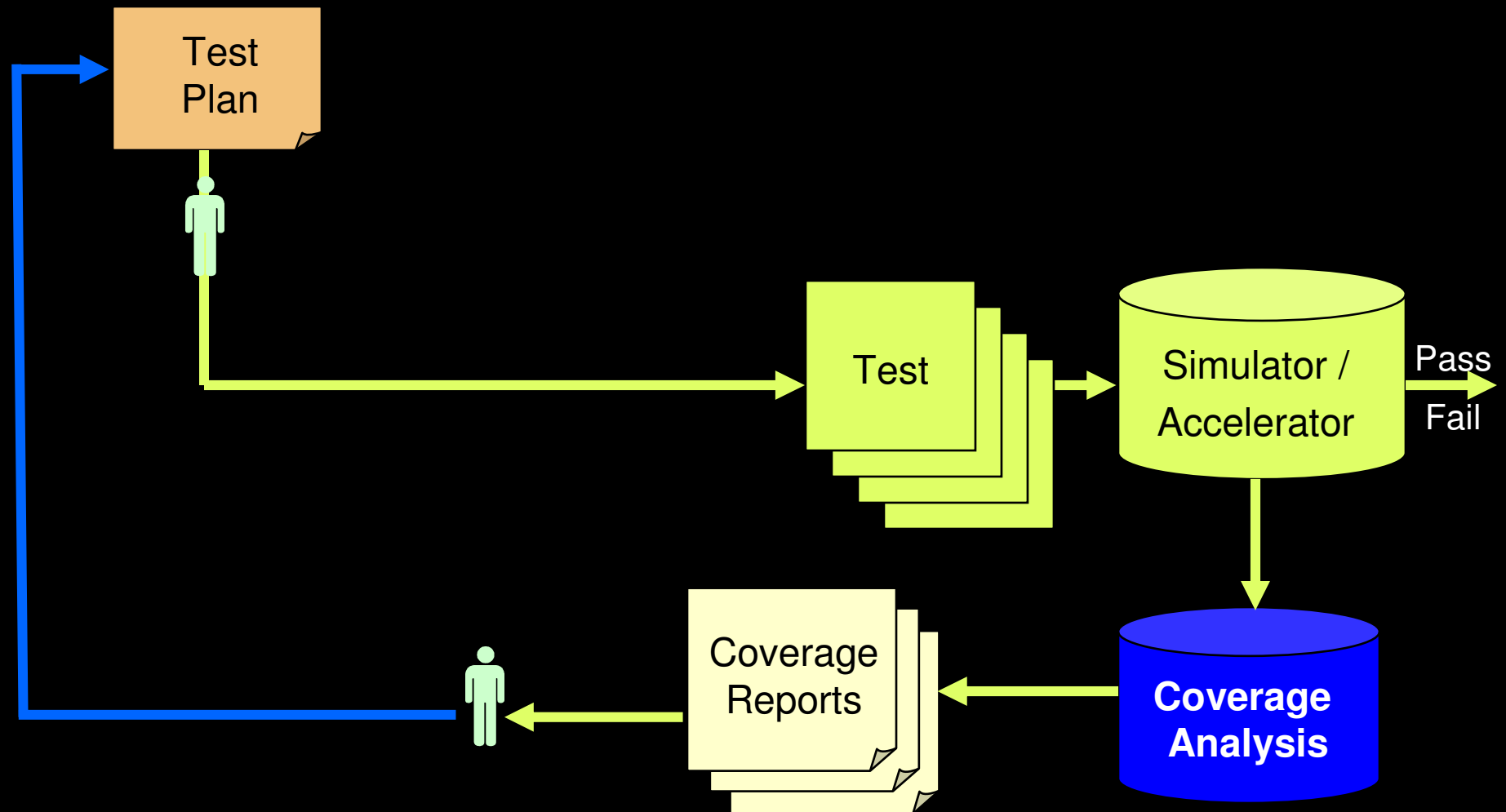
Amir Nahir, Allon Adir and Gil Shurek

12/11/2008

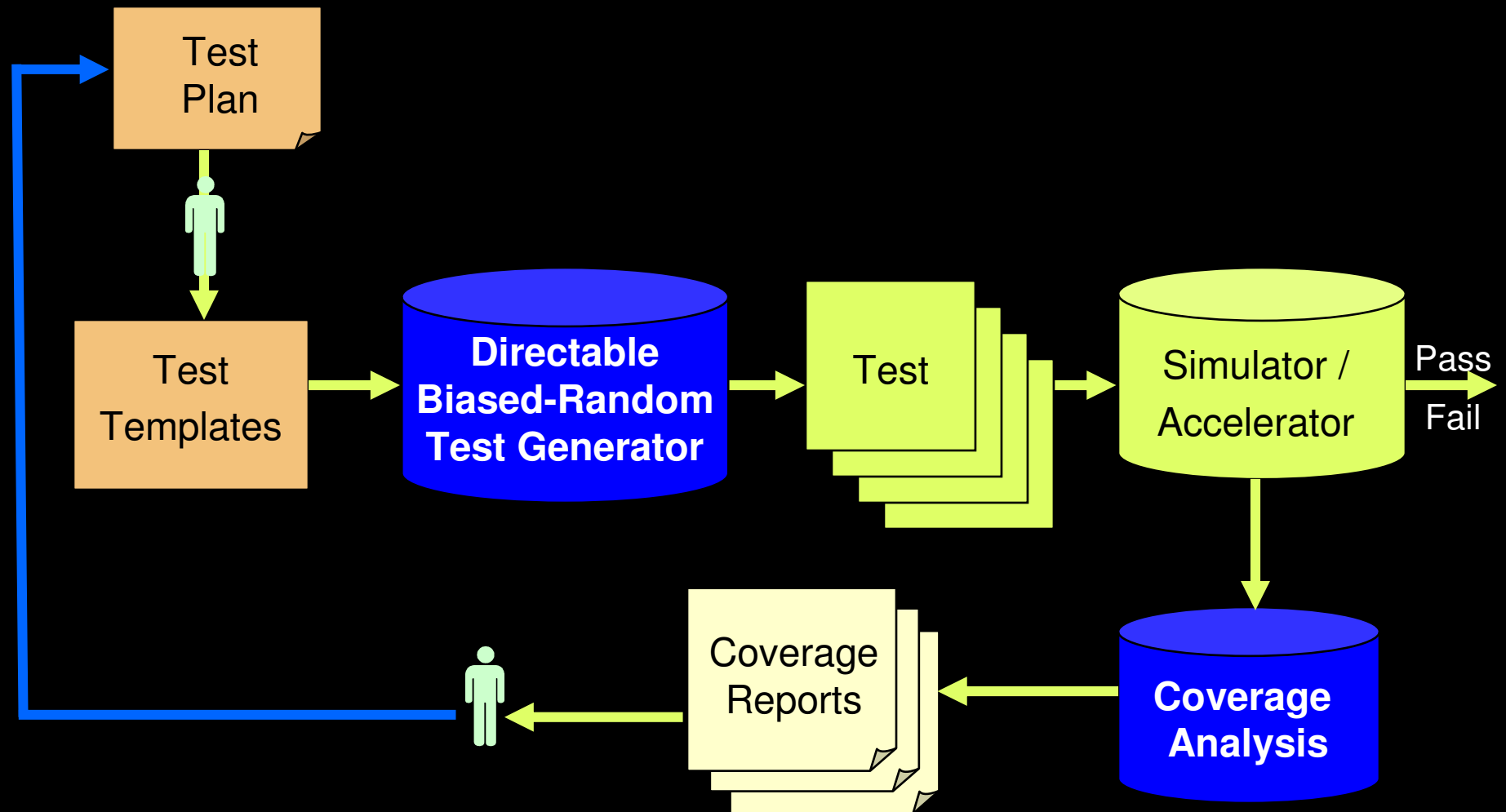
Agenda

- **Pre-silicon verification methodology**
 - And the accompanying technology
- **We'll never complete everything before tape-out**
- **Extending the pre-silicon methodology onto the silicon platform**
 - Technical challenges

Simulation-Based Functional Verification Flow



Simulation-based Directable Test Generation Methodology



Test Template Example

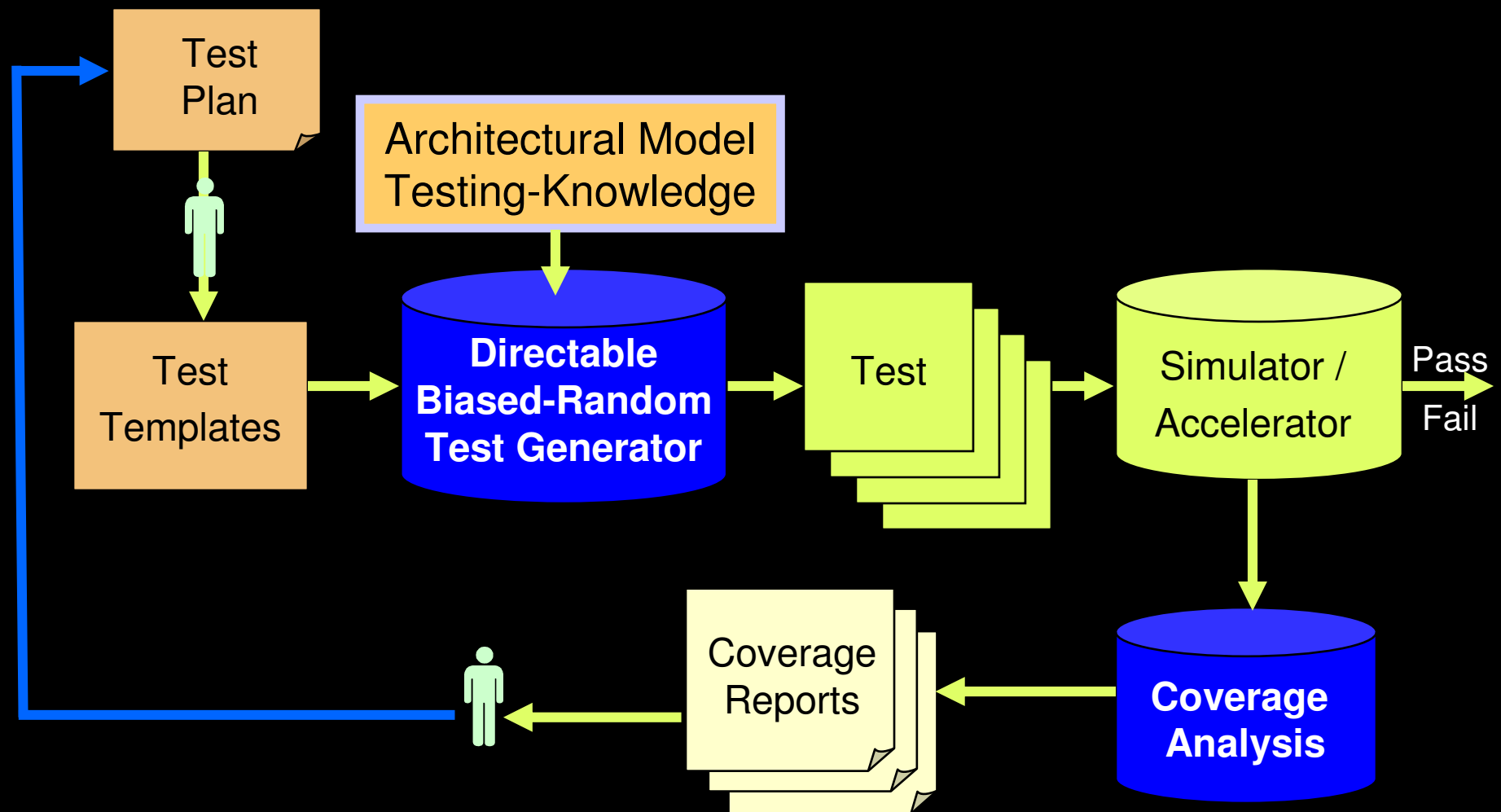
Genesys-Pro: Symmetric multi-processor test program generator from IBM

The screenshot displays the Genesys-Pro software interface. At the top is a menu bar with options: File, Edit, Insert, View, Tools, Windows, and Help. Below the menu bar is a toolbar with various icons for file operations, editing, and execution. The main window shows a table of test statements with columns: Statement, D, V, R, ?, !, &, Repeat, Mnemonic, Data RA, Code RA, and C. The table contains a sequence of statements: GPRODEF, CONCURRENT, PROCESS (0,0), lwa, One of, 10: stw, 10: lwa, PROCESS (0,1), and stw. The 'Repeat' column shows values #10 and [100,200]. The 'Mnemonic' column shows instructions like lwa __(\$A) and stw __(\$A). The 'Data RA' and 'Code RA' columns show 'editable'.

Statement	D	V	R	?	!	&	Repeat	Mnemonic	Data RA	Code RA	C
GPRODEF											
CONCURRENT											
PROCESS (0,0)											
lwa								lwa __(\$A)	editable	editable	
One of							#10				
10: stw								stw __(\$A)	editable	editable	
10: lwa								lwa __(\$A)	editable	editable	
PROCESS (0,1)											
stw							[100,200]	stw __(\$A)	editable	editable	

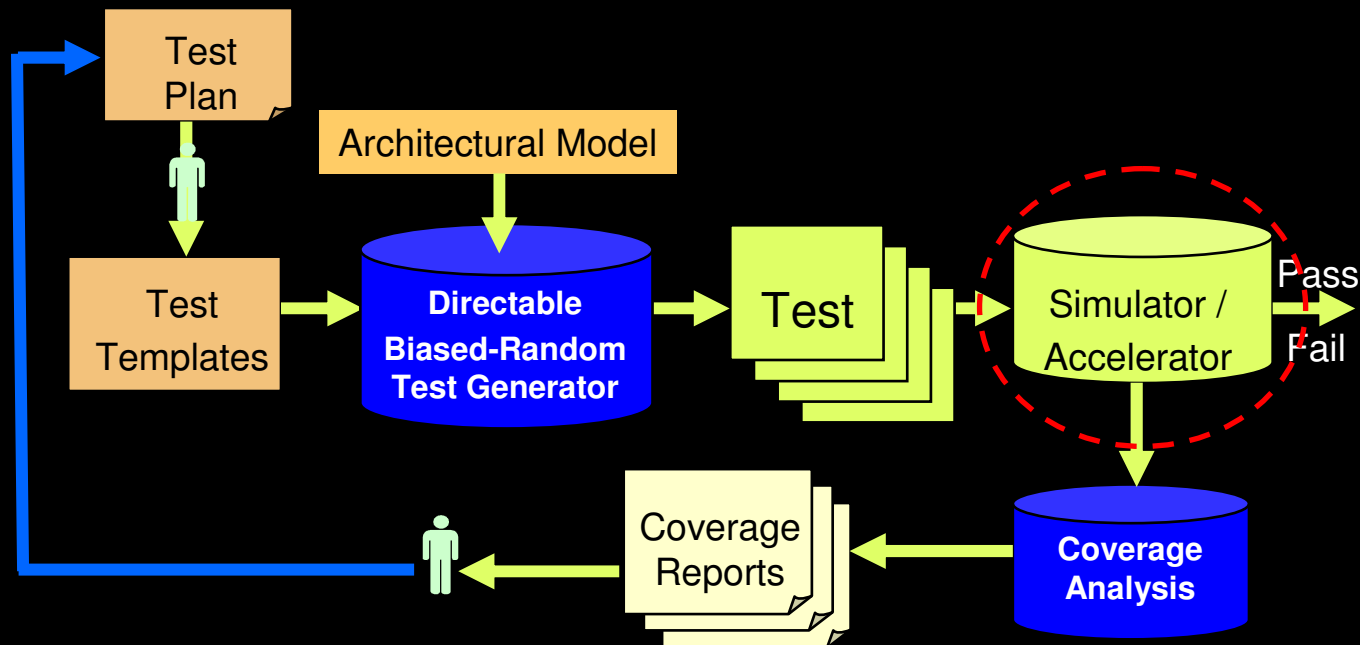
Architecture-Independent Test Program Generator

Ontology-driven



Platform Performance

~**500B** simulation cycles available to verify a processor
SW simulator with 10-100 cyc/sec : ~1500-150 years
HW accelerator with 10k-50k cyc/sec: 580-115 days
4GHz processor silicon : 125 sec

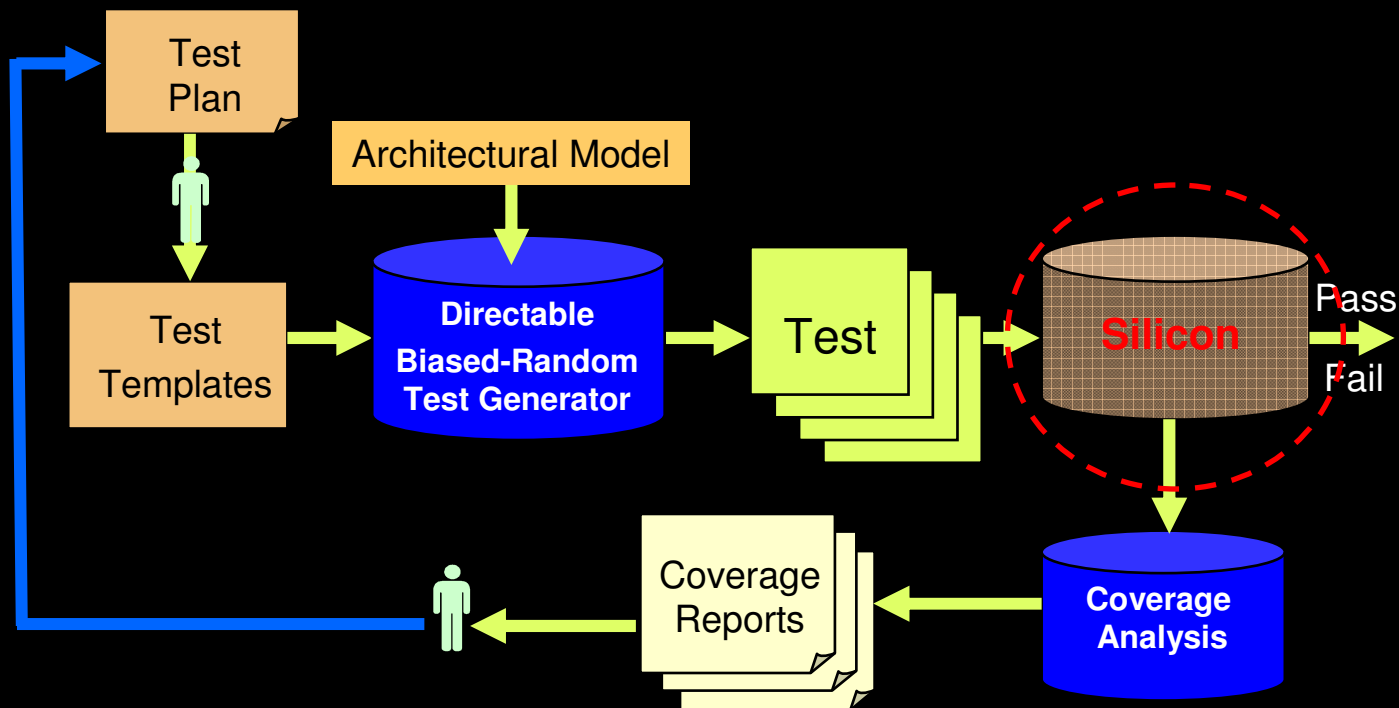


Platform Tradeoffs

	Software Simulation	Hardware Acceleration /Emulation	Hardware Bring-up
Performance	slow	faster	ideal speed
Control & Visibility	total model control/visibility	control/visibility with some penalty	very limited Per-instance checking
Price per platform unit	relatively inexpensive	expensive	very expensive as a functional verification platform

Can We Just Replace the Simulator with Silicon?

- High test loading/result offloading overhead \Rightarrow low silicon utilization
- Alternatively, need a program to run and check the results

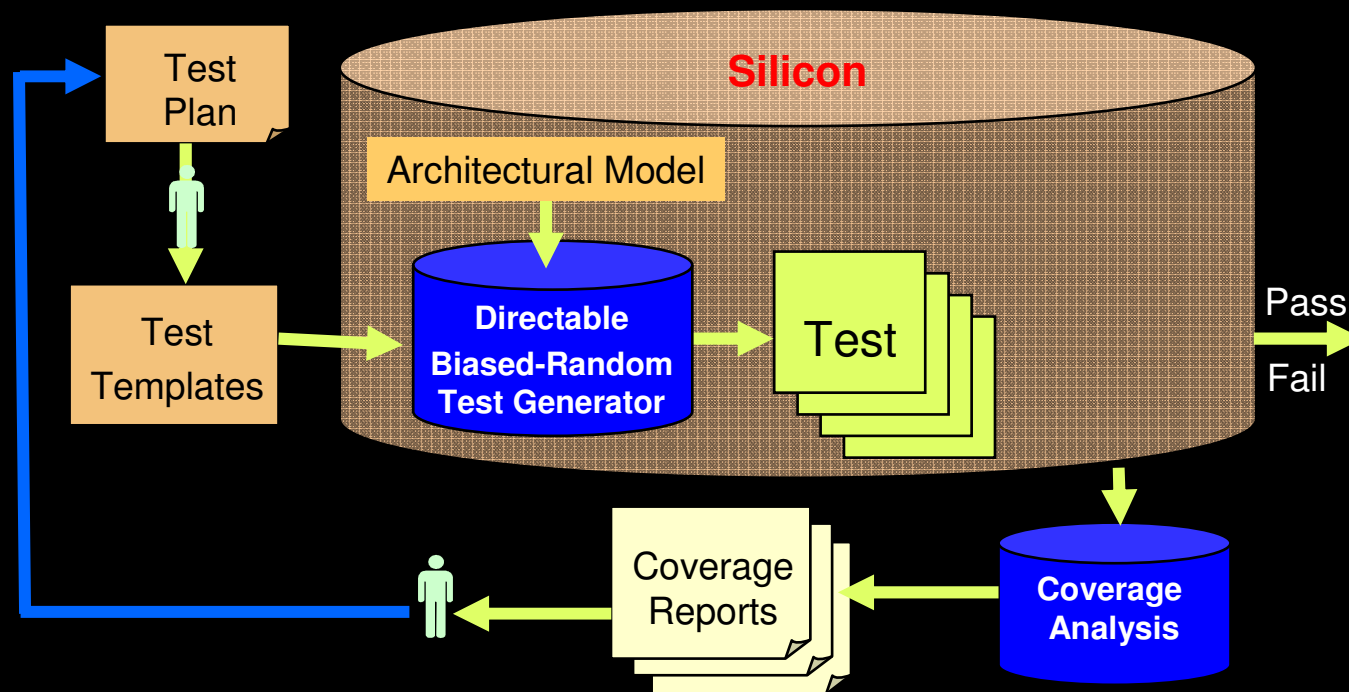


Hardware Exercisers

- A program that runs on the hardware and tests it
- Can take the form of a test program generator
 - Kept relatively simple to ensure high throughput
 - Simple enough to facilitate running and debugging on early bring-up
 - Bare metal: OS often not functional or not available
- Built-in checking
 - Self check – the test does what it's supposed to do
 - Run the test twice and compare results & behavior
 - Built-in reference model
- Practical Guide: “Random Test Generators for Microprocessor Design Validation”, Joel Storm, Sun Microsystems, EMICRO, 2006

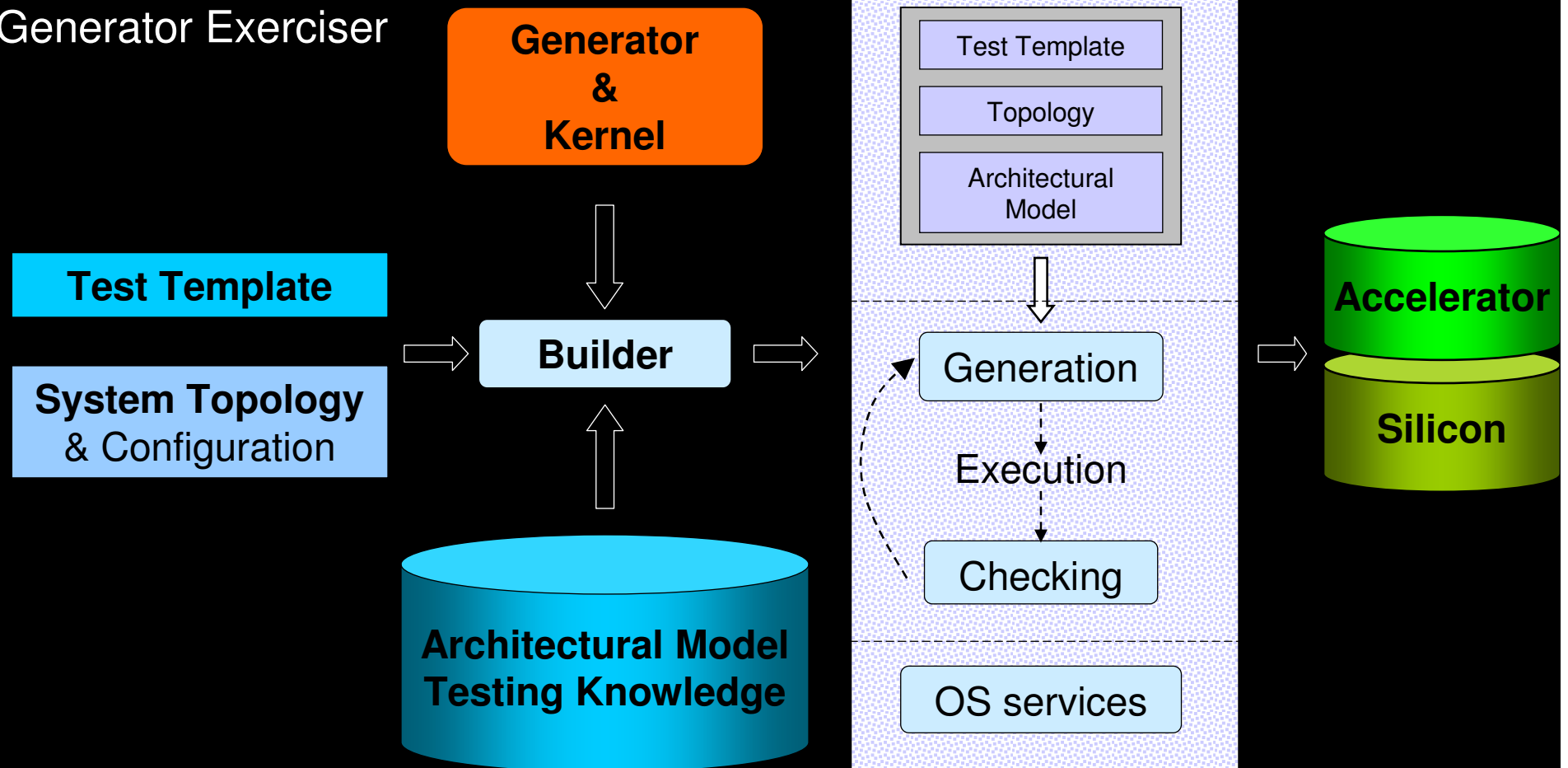
Can We Just Run the Generator as a HW Exerciser?

- Bare metal implies no file handling for templates/tests
- Need to keep the generator simple
- Need to handle the ontology

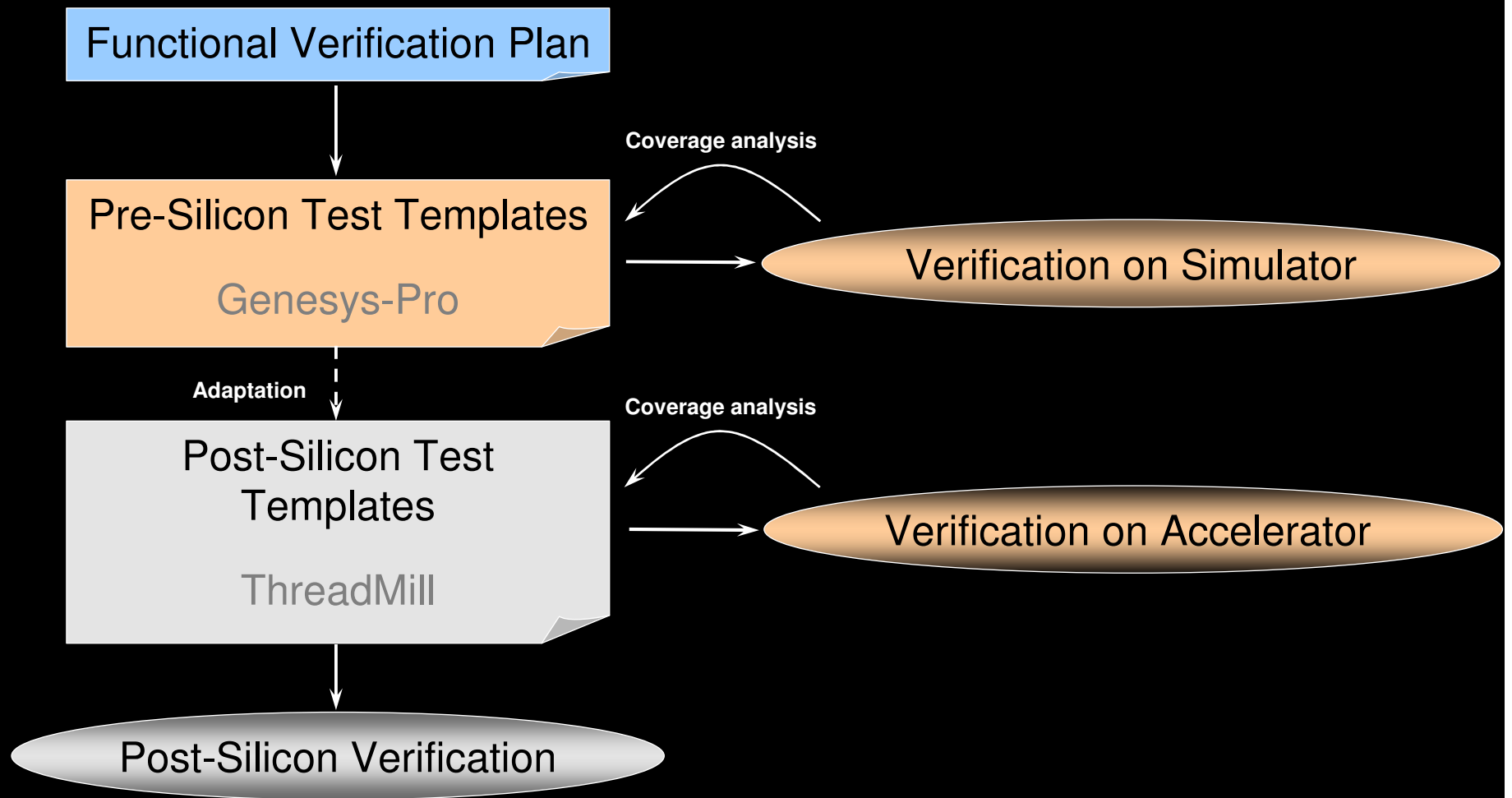


Architecture of a Directable Ontology-based Exerciser

ThreadMill: Symmetric Multi-Processor Test Program
Generator Exerciser



Cross-Platform Functional Verification Methodology



ThreadMill Usage

- Part of the functional verification of the next IBM Power processor
 - High-end server processor
 - Multi-processor, multi-threading
- Powerful test template language has proven effective for bug recreation on silicon
- Could also be used to assist production testing

Main Message

- A functional verification methodology based on
 - A simulation platform
 - A directable test program generator
 - A set of test templates covering the functional verification plan
 - Coverage measurement and feedback
- Can be extended from pre-silicon to post-silicon by the use of a directable exerciser



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Thank you

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